

Claims

1. An electronic structure having in-situ formed unit resistors comprising:

5 a pre-processed substrate having a first insulating material layer on top;

 a first plurality of conductive elements formed on said first insulating material layer;

10 a second insulating material layer overlying said first plurality of conductive elements and said first insulating material layer;

 a plurality of electrically resistive vias having a resistivity of at least 100 $\Omega\text{-cm}$ formed in said second insulating material layer wherein each of said first plurality of conductive elements in electrical communication with at least one of said 15 plurality of electrically resistive vias; and

 a second plurality of conductive elements formed on top of said second insulating material layer each in electrical communication with at least one of said plurality of electrically resistive vias.

Sub A2

2. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said pre-processed substrate is a semiconductor wafer having a first dielectric material layer on top.

5 3. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said pre-processed substrate is formed of an electrically insulating material selected from the group consisting of glass, ceramic and polymeric materials.

10 4. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias are formed of a refractory metal-silicon-nitrogen material.

15 5. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias are formed of a refractory metal-silicon-nitrogen material wherein the refractory metal is selected from the group consisting of Ta, Nb, V, W and Ti.

6. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias are formed of TaSiN having a composition of between about 10 at. % and about 55 at. % Ta, 5 between about 10 at. % and about 45 at. % Si, and between about 30 at. % and about 80 at. % N.

7. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias each has a diameter between about 0.1 10 μm and about 100 μm , and a height between about 10 nm and about 1,000 nm.

8. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias having a resistivity preferably of at 15 least 150 $\Omega\text{-cm}$.

9. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias are formed by depositing a TaSiN film layer into a plurality of via openings, wherein said TaSiN film 20 layer having a sheet resistance between about 0.3 M- Ω /square and about 1 M- Ω /square.

10. An electronic structure having in-situ formed unit resistors according to claim 9, wherein said sheet resistance is preferably between about 1 K- Ω /square and about 10 K- Ω /square.

11. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said plurality of electrically resistive vias having a diameter preferably of about 1 μm , and a height preferably of about 100 nm.

12. An electronic structure having in-situ formed unit resistors according to claim 1, wherein said first plurality of conductive elements and said second plurality of conductive elements are formed of a material selected from the group consisting of doped polysilicon, metal silicide, polycide, refractory metals, aluminum, copper, and alloys thereof.

13. An electronic structure having in-situ formed unit resistors according to claim 1, wherein each of said first plurality of conductive elements is in electrical communication with two of said plurality of electrically resistive vias that are immediately adjacent to each other.

14. An electronic structure having in-situ formed unit resistors according to claim 1, wherein each of said second plurality of conductive elements is in electrical communication with two of said plurality of electrically resistive vias that are
5 immediately adjacent to each other.

15. An electronic structure having in-situ formed unit resistors according to claim 1 further comprising:

10 a third insulating material layer overlying said second plurality of conductive elements and said second insulating material layer;

15 a second plurality of electrically resistive vias having a resistivity of at least 100 $\Omega\text{-cm}$ formed in said third insulating material layer wherein each of said second plurality of conductive elements in electrical communication with at least one of said second plurality of electrically resistive vias; and

a third plurality of conductive elements formed on top of said third insulating material layer each in electrical communication with at least one of said second plurality of electrically resistive vias;

20 whereby at least one of said second plurality of electrically resistive vias is in electrical communication with at least one of said first plurality of electrically resistive vias.

16. A method for forming a semiconductor structure with
in-situ unit resistors comprising the steps of:

providing a pre-processed substrate having a planar top
surface;

5 depositing a first insulating material layer on said
planar top surface of said pre-processed substrate;

forming a first plurality of conductive elements on said
first insulating material layer;

10 depositing a second insulating material layer on top of
said first plurality of conductive elements and said first
insulating material layer;

forming a plurality of via openings in said second
insulating material layer, each of said via openings exposing one
of said first plurality of conductive elements;

15 depositing an electrically resistive metal having a
resistivity of at least 100 $\Omega\text{-cm}$ into said plurality of via
openings forming a plurality of electrically resistive vias; and

20 forming a second plurality of conductive elements on top
of said second insulating material layer wherein each of said
second plurality of conductive elements in electrical communication
with at least one of said plurality of electrically resistive vias.

17. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of depositing said electrically resistive metal in TaSiN.

5 18. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of depositing said electrically resistive metal by sputtering a Ta-Si alloy target in the presence of nitrogen.

10 19. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of depositing said electrically resistive metal by co-sputtering from Ta and Si targets in the presence of nitrogen.

15 20. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of depositing said electrically resistive metal by co-sputtering from a Ta target at a sputtering power of at least 50 W dc and a Si target at a sputtering power of at least 300 W rf.

20 21. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of depositing said electrically resistive metal by evaporation or chemical vapor deposition.

22. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of patterning a layer of said electrically resistive metal by reactive ion etching (RIE) utilizing a photoresist mask.

5 23. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 22 further comprising the step of conducting said RIE by using a gas of Cl_2/O_2 or Cl_2 .

10 24. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of forming said plurality of via openings each having a height between about 10 nm and about 1,000 nm, a diameter between about 0.1 μm and about 100 μm .

15 25. A method for forming a semiconductor substrate with in-situ unit resistors according to claim 16 further comprising the step of removing excess electrically resistive metal from a top surface of said second insulating material layer by chemical mechanical polishing.

26. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor comprising:

a unit resistor formed by a first conductive element and
5 a second conductive element situated in different levels in said electronic structure connected therein-between by an electrically resistive via, said electrically resistive via being formed of a material having a resistivity of at least 100 Ω-cm; and

10 a capacitor formed juxtaposed to and in electrical communication with said unit resistor.

27. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said capacitor being a deep-trench capacitor or a stacked capacitor.

15 28. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said unit resistor being electrically connected to in-series with said capacitor.

29. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said unit resistor being electrically connected in-parallel with said capacitor.

5 30. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said unit resistor being electrically connected to and situated on top of said capacitor.

10 31. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said unit resistor being electrically connected to and situated below said capacitor.

15 32. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said electrically resistive via being formed of a refractory metal-silicon-nitrogen material wherein said refractory metal is selected from the group consisting of Ta, Nb, V, W and Ti.

33. An electronic structure having an in-situ formed unit resistor in electrical communication with a capacitor according to claim 26, wherein said electrically resistive via being formed of a diameter between about 0.1 μm and about 100 μm ,
5 and a height between about 10 nm and about 1,000 nm.